

Features

- Excellent thermal stability
- Common source configuration
- Broadband performances $P_{OUT} = 2\text{ W}$ with 13 dB gain @ 870 MHz
- Plastic package
- ESD protection
- Supplied in tape and reel
- In compliance with the 2002/95/EC european directive

Description

The PD84002 is a common source N-channel, enhancement-mode lateral Field-Effect RF power transistor. It is designed for high gain, broad band commercial and industrial applications. It operates at 7 V in common source mode at frequencies of up to 1 GHz.

PD84002's superior gain and efficiency makes it an ideal solution for portable radio and UHF RFID reader.

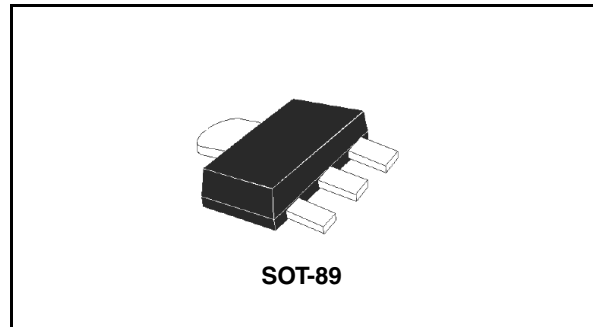


Figure 1. Pin connection

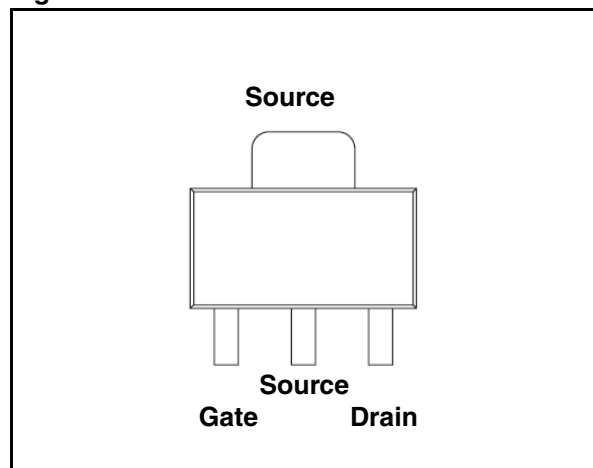


Figure 2. Device summary

| Order code | Marking | Package | Packaging |
|------------|---------|---------|---------------|
| PD84002 | 8402 | SOT-89 | Tape and reel |

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1 Electrical data

1.1 Maximum ratings

Table 1. Absolute maximum ratings ($T_{CASE} = 25^{\circ}C$)

| Symbol | Parameter | Value | Unit |
|---------------|-------------------------------------|-------------|-------------|
| $V_{(BR)DSS}$ | Drain-source voltage | 25 | V |
| V_{GS} | Gate-source voltage | -0.5 to +15 | V |
| I_D | Drain current | 2 | A |
| P_{DISS} | Power dissipation | 6 | W |
| T_J | Max. operating junction temperature | 150 | $^{\circ}C$ |
| T_{STG} | Storage temperature | -65 to +150 | $^{\circ}C$ |

1.2 Thermal data

Table 2. Thermal data

| Symbol | Parameter | Value | Unit |
|------------|------------------------------------|-------|---------------|
| R_{thJC} | Junction - case thermal resistance | 21 | $^{\circ}C/W$ |

2 Electrical characteristics

$$T_{CASE} = +25\text{ }^{\circ}\text{C}$$

2.1 Static

Table 3. Static

| Symbol | Test conditions | | Min | Typ | Max | Unit |
|--------------|-------------------------|-------------------------|-----|------|-----|---------------|
| I_{DSS} | $V_{GS} = 0\text{ V}$ | $V_{DS} = 25\text{ V}$ | | | 1 | μA |
| I_{GSS} | $V_{GS} = 5\text{ V}$ | $V_{DS} = 0\text{ V}$ | | | 1 | μA |
| $V_{GS(Q)}$ | $V_{DS} = 7.5\text{ V}$ | $I_D = 100\text{ mA}$ | | 3.9 | | V |
| $V_{DS(ON)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 0.25\text{ A}$ | | 0.27 | | V |
| C_{ISS} | $V_{GS} = 0\text{ V}$ | $V_{DS} = 7.5\text{ V}$ | | 16 | | pF |
| C_{OSS} | $V_{GS} = 0\text{ V}$ | $V_{DS} = 7.5\text{ V}$ | | 16 | | pF |
| C_{RSS} | $V_{GS} = 0\text{ V}$ | $V_{DS} = 7.5\text{ V}$ | | 1.2 | | pF |

2.2 Dynamic

Table 4. Dynamic

| Symbol | Test conditions | Min | Typ | Max | Unit |
|---------------|--|------|-----|-----|------|
| P_{OUT} | $V_{DD} = 7.5\text{ V}$, $I_{DQ} = 100\text{ mA}$, $P_{IN} = 0.1\text{ W}$, $f = 870\text{ MHz}$ | 2 | | | W |
| G_{PS} | $V_{DD} = 7.5\text{ V}$, $I_{DQ} = 100\text{ mA}$, $P_{OUT} = 2\text{ W}$, $f = 870\text{ MHz}$ | 13 | 15 | | dB |
| N_D | $V_{DD} = 7.5\text{ V}$, $I_{DQ} = 100\text{ mA}$, $P_{OUT} = 2\text{ W}$, $f = 870\text{ MHz}$ | 60 | 65 | | % |
| Load mismatch | $V_{DD} = 7.5\text{ V}$, $I_{DQ} = 100\text{ mA}$, $P_{OUT} = 2\text{ W}$, $f = 870\text{ MHz}$ All phase angles | 20:1 | | | VSWR |

2.3 ESD protection characteristics

Table 5. ESD protection characteristics

| Test conditions | Class |
|------------------|-------|
| Human body model | 2 |
| Machine model | M3 |

2.4 Moisture sensitivity level

Table 6. Moisture sensitivity level

| Test methodology | Rating |
|------------------|--------|
| J-STD-020B | MSL 3 |

3 Impedances

Figure 3. Impedances

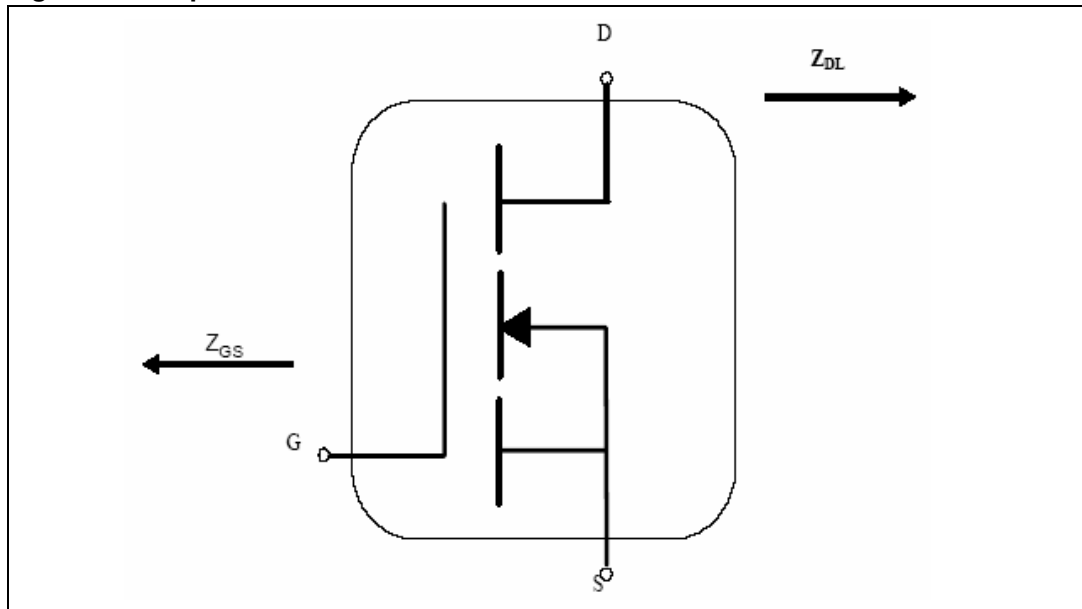


Table 7. Impedances

| F(MHz) | Z_{GS} | Z_{DL} |
|--------|-----------------|-----------------|
| 860 | $1,80 + j 7,79$ | $3,88 + j 2,41$ |
| 870 | $1,84 + j 7,96$ | $3,89 + j 2,69$ |
| 880 | $1,83 + j 8,01$ | $4,01 + j 2,96$ |
| 890 | $1,76 + j 8,11$ | $4,17 + j 3,16$ |
| 900 | $1,70 + j 8,20$ | $4,27 + j 3,32$ |
| 910 | $1,63 + j 8,30$ | $4,37 + j 3,40$ |
| 920 | $1,57 + j 8,48$ | $4,41 + j 3,46$ |
| 930 | $1,43 + j 8,64$ | $4,36 + j 3,51$ |
| 940 | $1,41 + j 8,83$ | $4,28 + j 3,51$ |

4 DC curves

Figure 4. DC output characteristics

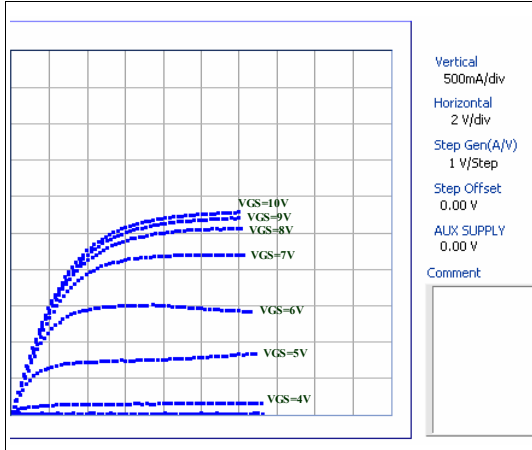


Figure 5. ID vs VGS

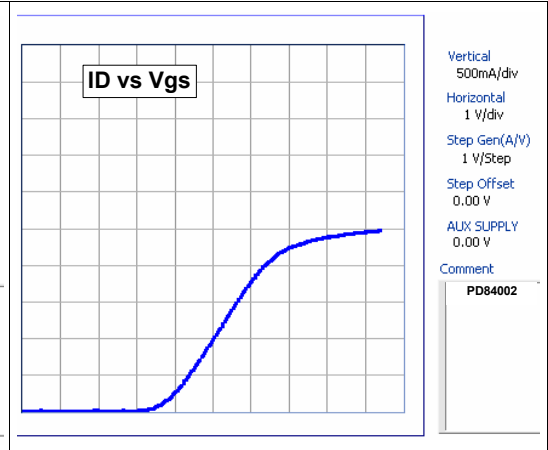
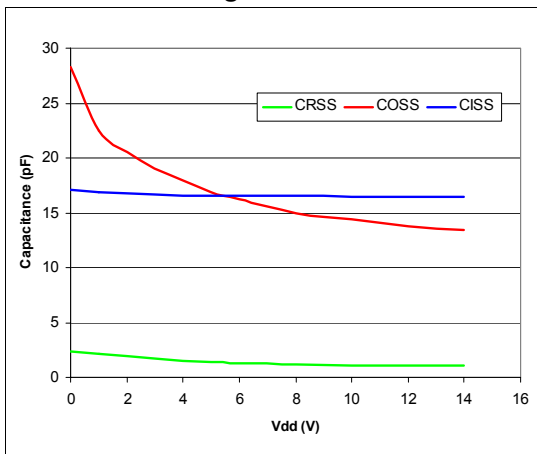


Figure 6. Capacitances vs drain voltage



5 RF curves

Figure 7. Output power and efficiency vs frequency 7.2 V / 100 mA / Pin = 19 dBm

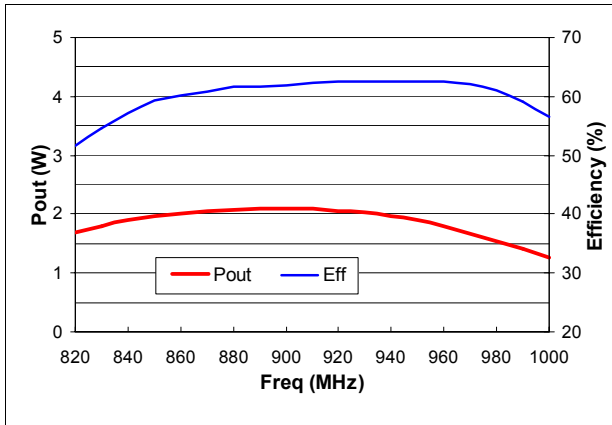


Figure 8. Gain vs frequency 7.2 V - 100 mA

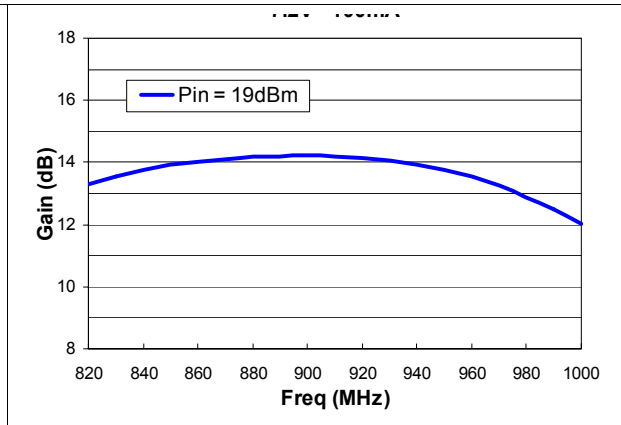


Figure 9. Input return loss vs frequency 7.2 V / 100 mA

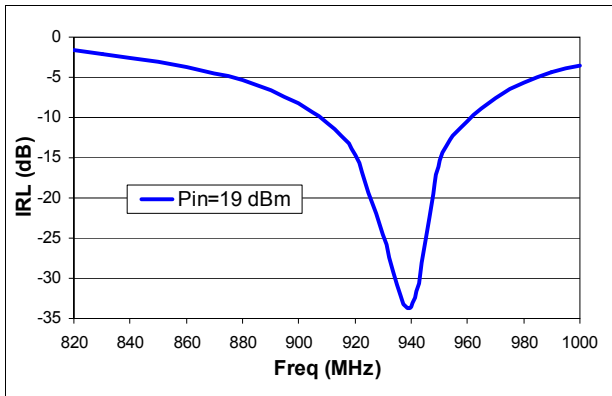


Figure 10. Harmonics vs frequency 7.2 V / 100 mA

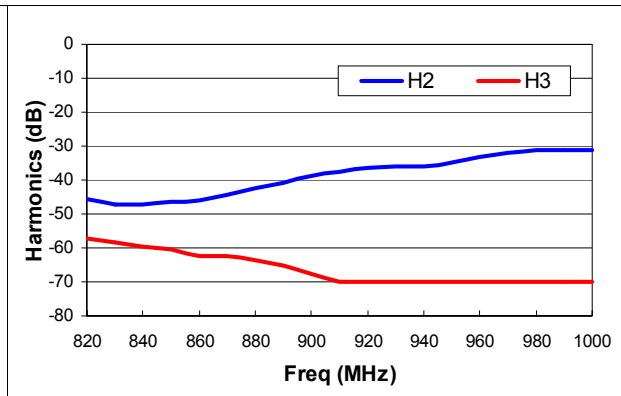
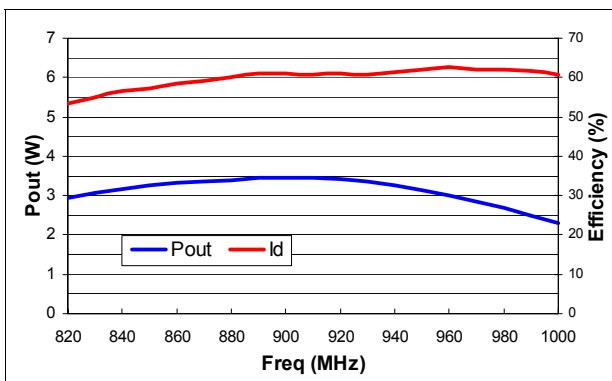


Figure 11. Output power and efficiency vs frequency 9 V / 100 mA / Pin = 22 dBm



6 Schematic and BOM

Figure 12. Schematic

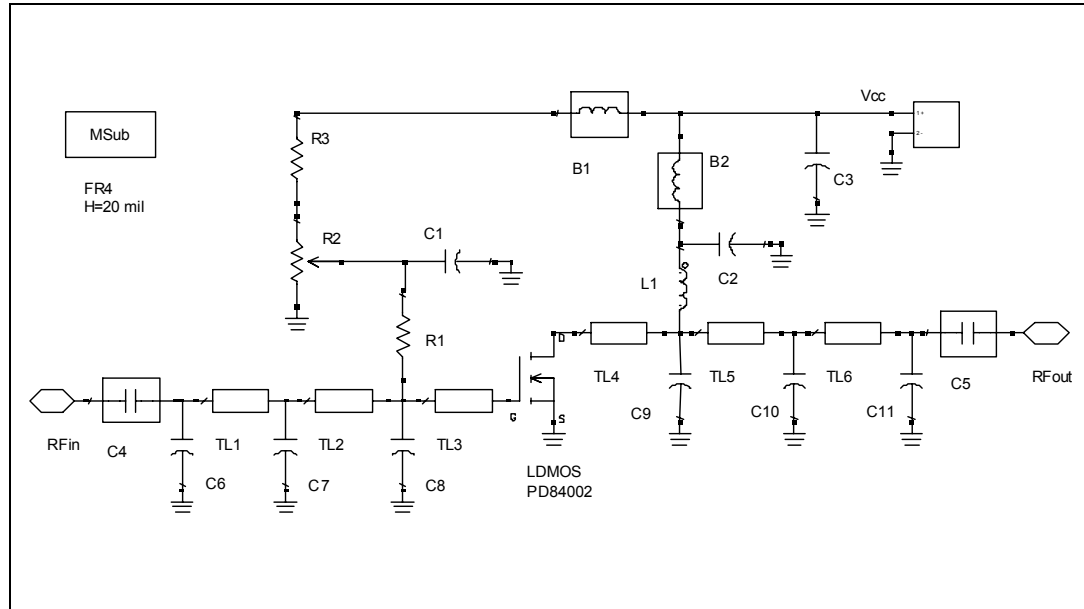


Table 8. Components part list

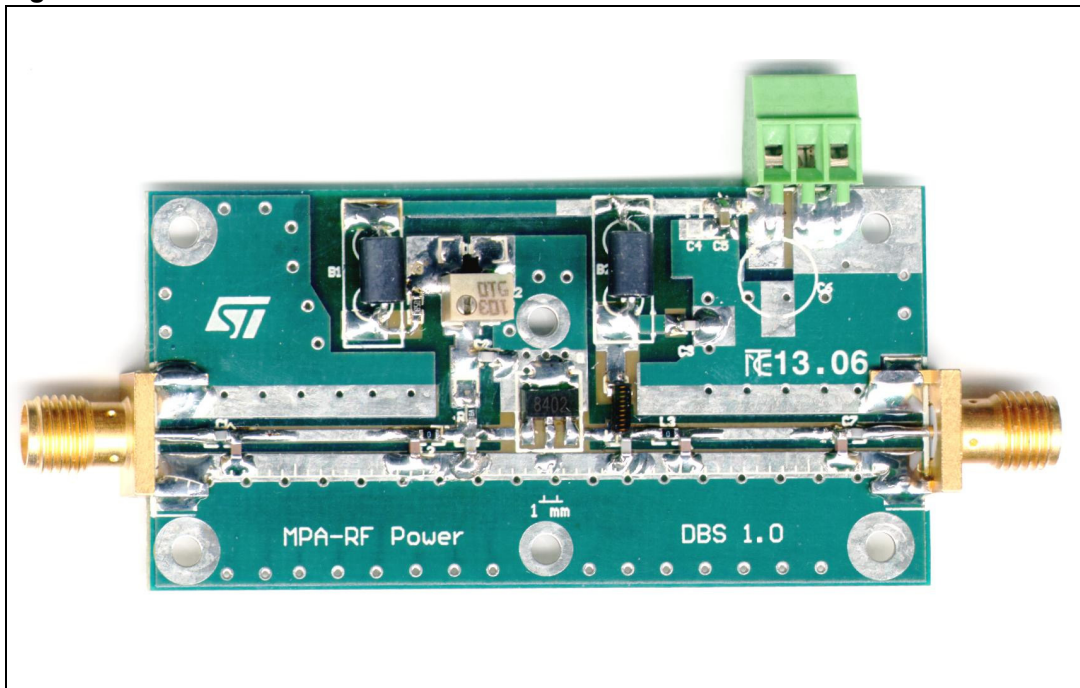
| Component ID | Description | Value | Case size | Manufacturer | Part Code |
|--------------|---------------|----------|-----------|--------------------|---------------------|
| B1 | Ferrite Bead | | | Panasonic | EXCELDR35C |
| B2 | Ferrite Bead | | | Panasonic | EXCELDR35C |
| C1, C2 | Capacitor | 120 pF | 0603 | Murata | GRM39-C0G121J50D500 |
| C3 | Capacitor | 1 uF | 0603 | Murata | GRM39-X5R105K16D52K |
| C4, C5 | Capacitor | 39 pF | 0603 | Murata | GRM39-C0G390J50D500 |
| C6, C10 | Capacitor | 3.3 pF | 0603 | Murata | GRM39-C0G3R3C50Z500 |
| C7 | Capacitor | 8.2 pF | 0603 | Murata | GRM39-C0G8R2D50Z500 |
| C8 | Capacitor | 22 pF | 0603 | Murata | GRM39-C0G220J50D500 |
| C9 | Capacitor | 12 pF | 0603 | Murata | GRM39-C0G120J50D500 |
| C11 | Capacitor | 2.7 pF | 0603 | Murata | GRM39-C0G2R7C50Z500 |
| L1 | Inductor | 12.55 nH | | Coilcraft | 1606-10 |
| R1 | Resistor | 150 Ω | 0603 | Tyco electronics | |
| R2 | Potentiometer | 10 KΩ | | Bourns electronics | 3214W-1-103E |
| R3 | Resistor | 1 K | 0603 | Tyco electronics | 01623440-1 |

Table 8. Components part list (continued)

| Component ID | Description | Value | Case size | Manufacturer | Part Code |
|---------------|-----------------------------------|-----------|-----------|--------------------|--------------|
| TL1 | Transmission line | W=0.92 mm | L=13.6 mm | | |
| TL2 | Transmission line | W=0.92 mm | L=3.5 mm | | |
| TL3 | Transmission line | W=0.92 mm | L=4.2 mm | | |
| TL4 | Transmission line | W=0.92 mm | L=3.8 mm | | |
| TL5 | Transmission line | W=0.92 mm | L=3.7 mm | | |
| TL6 | Transmission line | W=0.92 mm | L=11.3 mm | | |
| RF in, RF out | SMA-CONN | 50 Ω | 60 mils | JOHNSON | 142-0701-801 |
| PD84002 | LDMOS | | | STMicroelectronics | PD84002 |
| Board | FR-4 THk=0.020" 2OZ Cu Both Sides | | | | |

7 Photo

Figure 13. Photo



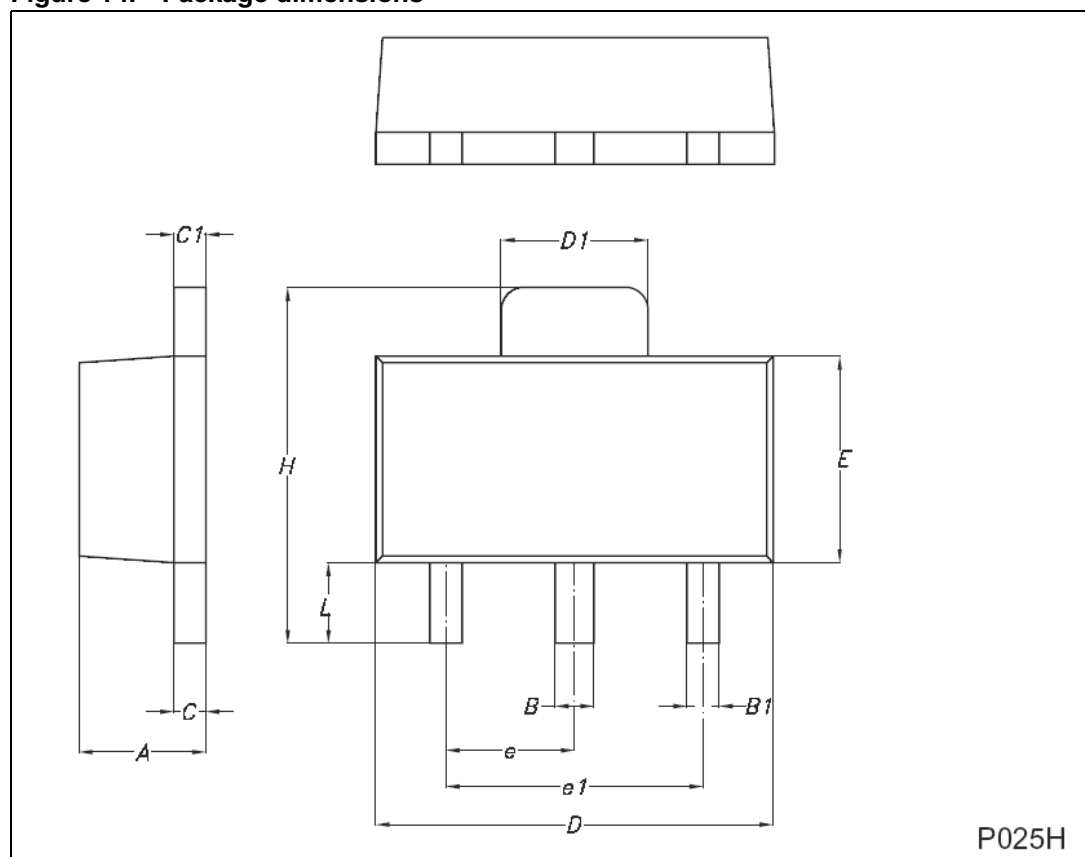
8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 9. SOT-89 mechanical data

| Dim. | mm. | | | Inch | | |
|------|------|-----|------|-------|-----|-------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 1.4 | | 1.6 | 55.1 | | 63.0 |
| B | 0.44 | | 0.56 | 17.3 | | 22.0 |
| B1 | 0.36 | | 0.48 | 14.2 | | 18.9 |
| C | 0.35 | | 0.44 | 13.8 | | 17.3 |
| C1 | 0.35 | | 0.44 | 13.8 | | 17.3 |
| D | 4.4 | | 4.6 | 173.2 | | 181.1 |
| D1 | 1.62 | | 1.83 | 63.8 | | 72.0 |
| E | 2.29 | | 2.6 | 90.2 | | 102.4 |
| e | 1.42 | | 1.57 | 55.9 | | 61.8 |
| e1 | 2.92 | | 3.07 | 115.0 | | 120.9 |
| H | 3.94 | | 4.25 | 155.1 | | 167.3 |
| L | 0.89 | | 1.2 | 35.0 | | 47.2 |

Figure 14. Package dimensions

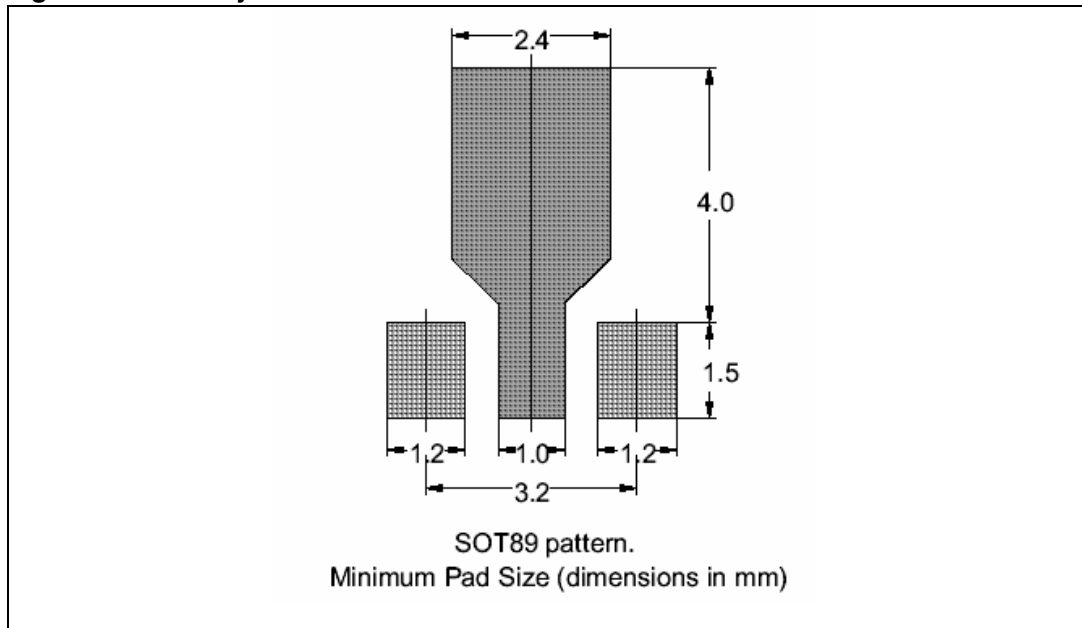


8.1 Thermal pad and via design

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device.

The via pattern is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025 plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

Figure 15. Pad layout details



8.2 Soldering profile

Figure 16 shows the recommended solder for devices that have Pb-free terminal plating and where a Pb-free solder is used.

Figure 16. Recommended solder profile

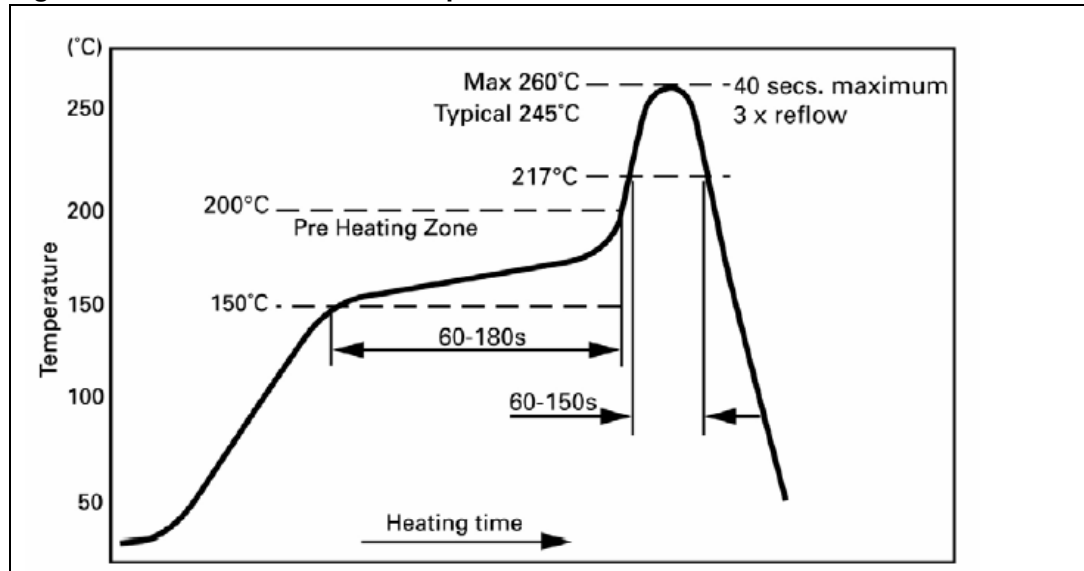


Figure 17 shows the recommended solder for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 17. Recommended solder profile for leaded devices

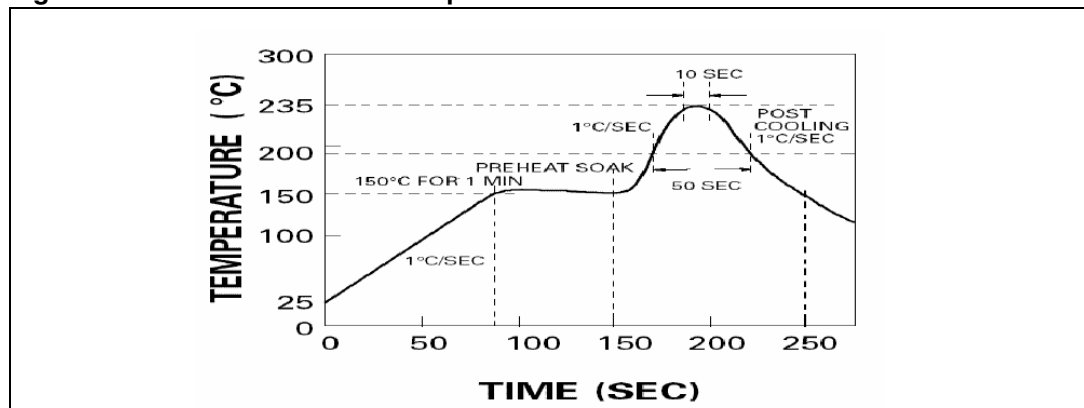
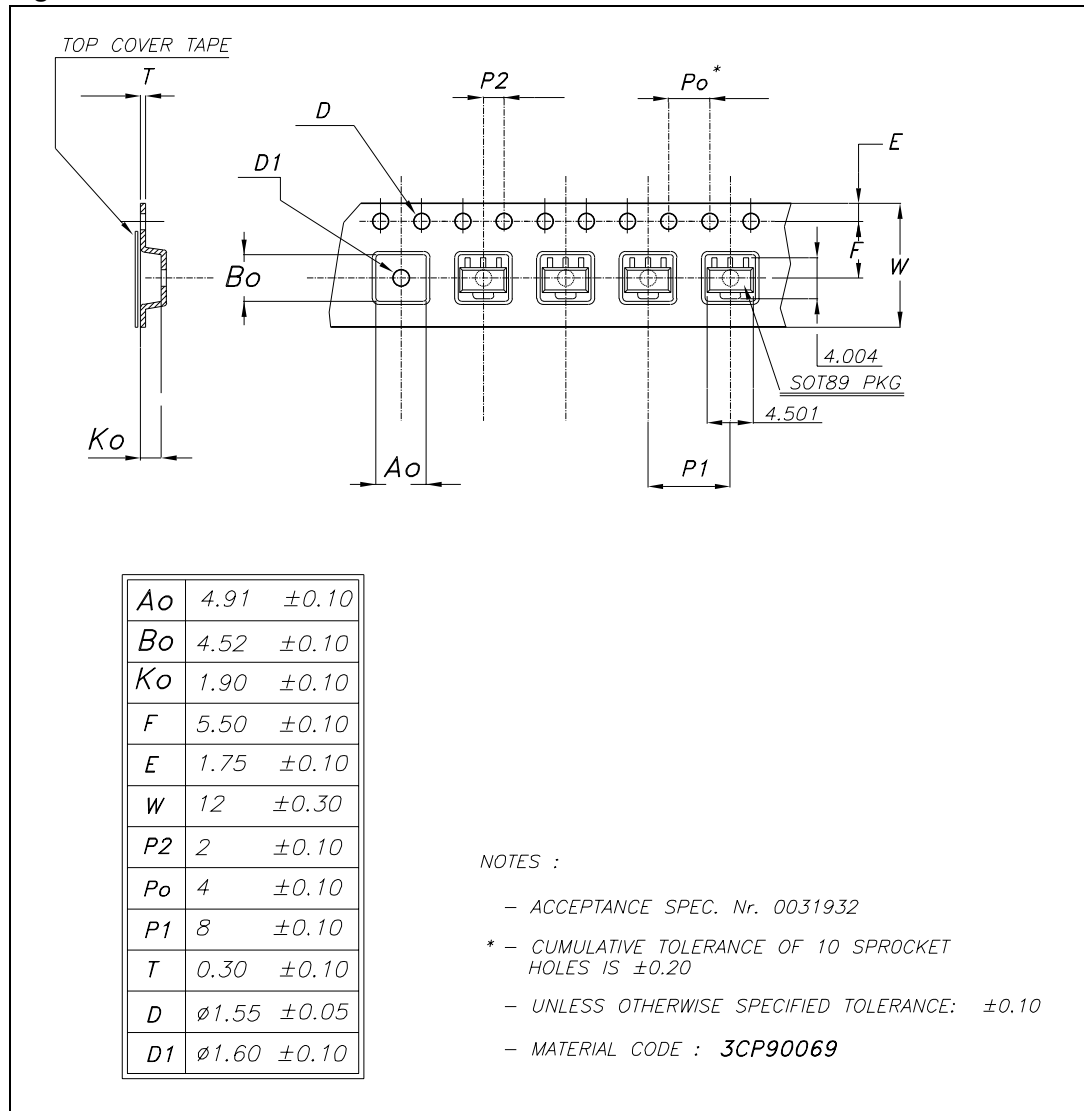


Figure 18. Reel information



9 Revision history

Table 10. Document revision history

| Date | Revision | Changes |
|-------------|----------|------------------|
| 05-Dec-2007 | 1 | Initial release. |

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